Prototype TDI sensors in embedded CCD in CMOS technology

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Abstract: This paper describes prototype time-delay-integration (TDI) sensors designed at Imec under CNES (French Space Agency) contract. The sensors combine a light-sensitive embedded CCD TDI section with a CMOS readout multiplexer on the same die and, fabricated using a modified 130nm CMOS-CIS technology.

Introduction: In imaging applications where either the sensor or the target is in constant relative motion, a one dimensional sensor can be used to generate a two dimensional image of the scene. A linear sensor however, has to trade resolution with signal-to-noise ratio (SNR). To overcome this limit, TDI mode of operation can be used, in which light from target is accumulated by multiple unit cells. An ideal n-stage TDI will increase the SNR by $\sqrt{n}$ without sacrificing resolution [1].

TDI mode of operation can be implemented with active pixel sensors, where signals from different unit cells can be read-out and summed in sync with the motion either in analog or digital domain [2, 3, 4]. The requirement that total noise introduced during readout and summation must be low makes these implementations difficult. On the other hand, sensors utilizing charge shift registers (bucket brigades and CCDs) offer a natural way to implement TDI, as motion of the charge pockets can be made to match scene motion. With a properly designed CCD, TDI processing can be essentially noiseless. This performance is difficult to match with the active pixels.

CCD technology (oxide thickness/voltages) does not follow CMOS scaling hence monolithic sensors that could combine the noise-free TDI implementation advantage of CCDs with the integration advantage of modern CMOS technologies were lacking. Hybrid approaches [5] could offer excellent performance, but cost/complexity prohibits their wide utilization. There has been recent interest in combining modern sub-micron CMOS technology with CCDs on the same die [6, 7, 8, 9, 10]. In this paper we describe a novel CCD module embedded into 130nm CMOS/CIS technology to answer this need, and prototype TDI sensors fabricated with this technology for aerospace push-broom applications.

In addition to traditional TDI imaging applications [11] (high-speed/resolution inspection/scanning), embedded CCD TDI functionality could also be utilized on the read out integrated circuits (ROIC) for hybrid infrared [12] and x-ray [13] imagers, where it could offer an alternative to switched capacitor [14] and bucket-brigade [15] implementations. Apart from TDI, low-noise/leakage sampling capability of CCDs can be used to implement dense analog memory elements for high-speed burst imagers [6, 43] and for high energy physics front-end electronics [16]. Computational imagers [10] and scientific imagers which have to accumulate very small (typically below read-noise) signals from repetitive experiments [17] could also benefit from this technology.

This paper is organized as follows. We first present Imec's embedded CCD technology. This is followed by TDI sensor implementation. As primary operating environment of the sensors is space, radiation sensitivity issues are briefly discussed next, followed by conclusions.

CCD Module Device Design: CCD and CMOS devices were integrated on the same die, during early 80s where CCDs were still utilized in non-imaging applications [18-20]. Recent utilization of embedded CCDs focused primarily on imaging applications [6, 7, 10, 21, 22]. CCDs traditionally use oxide/nitride stacks with thicknesses on the order of 70-150nm, and operating voltages around 5-12V. Imec's CCD module uses a single, 3.3V compatible oxide for both CMOS and CCD modules. This choice is done primarily to have an embedded CCD module that can be used with CMOS compatible voltages and possibly in combination with the existing pinned photodiode (PPD) technology [23]. The CCD module utilizes a single, non-overlapping poly-silicon layer. Similar non-overlapping electrodes have been used on horizontal registers of video CCDs. Those approaches either used gaps of approx. 250-300nm in combination with inter-gap implants to control inter-electrode pocket sizes [24, 25] or very narrow gaps with no additional inter-gap implants [26]. We followed the latter approach: Figure 1 shows the narrow gap (120nm) electrode implementation.

To reduce the risk of charge transfer efficiency degradation with radiation damage, and also to enable other high-speed applications, we targeted buried channel CCDs, where additional n-implants are used to define channel regions away from silicon/oxide interface. Channel depth [27] and dose [28] are chosen via TCAD to ensure a charge capacity of a few Ke-/um^2, and 99.99% transfer efficiency in a transfer time of < 100nsec for the largest electrode size planned. This relaxed transfer efficiency value is justified by the limited length of the TDI CCD chain

With the CMOS voltages limited to 3.3V, a method to couple electrons from deeper CCD wells to CMOS levels is needed. One approach is to transfer the charges to a properly sized surface channel CCD just before dumping to electrometer diffusion. This transition can be accomplished, for example by engineering buried channel implants, or by using a fat-zero like approach [29]. Another possible solution is to boost the electrometer diffusion potential via bootstrapping. The scheme we utilized is explained on figure 2, where additional light-shielded transition electrodes operated in the pinned surface channel mode are used. The draw-backs of this approach are increased capacitive load on

the blocking electrode and possibly long charge transfer times for large charge pockets.

CCD Module Integration: Deep submicron CMOS technologies utilize shallow trench isolation (STI), which must maintain a certain density to prevent incomplete oxide removal or nitride over-etch during front-end processing. CCDs on the other hand, contain very large active areas devoid of any structures, hence CCD integration requires adapting the STI module for defect free implementation. To push the channel charges away from silicon-oxide interfaces, the STI edges must also be doped. To reduce risk of electrode-electrode shorts, the poly module must be modified. Additionally, the poly doping steps must be adjusted to maintain uniform buried channel doping. The silicide and contact rules must be modified to eliminate risk of silicide bridges. For front-side illumination (FSI) applications, the silicide in the CCD must be blocked. For large FSI CCD arrays, the back-end metal density will also be much lower than typical CMOS targets. In this case the back-end modules must be tuned to ensure planarity and good contact/via yield. All of these process changes have been implemented in Imec's 130 nm CMOS-CIS technology.

TDI Sensor CCD Core: Industrial TDI sensors utilize pixel sizes ranging from 5um to 30um and line rates in excess of 100 KHz. To achieve high SNR with min. number of TDI steps, a high QE is desired. Electrode reticulation [30], thinning [31], transparent electrodes [32], or back-side illumination (BSI) approaches can be used. We targeted the latter: Prototype sensors are design for FSI but all technology and sensor decisions are made with back-side processing and operational compatibility in mind. For the TDI sensor unit cell following options were considered: (1) CCD both as photo-sensor and transfer, (2) CCD with overflow protection, (3) PPD coupled to transfer CCD, (4) PPD coupled to transfer CCD with overflow protection. (3) and (4) offer better FSI QE, however they require complex unit cells with limited fill-factor(FF)/full-well, and are also harder to scale. (2) and (4) offer anti-blooming (AB) functionality, which is important for aerospace TDI applications. For the prototypes we designed unit cell types (1) and (2). For the overflow functionality, following options considered: (i) vertical AB schemes similar to those utilized on IL-video CCDs, lateral AB with (ii) implanted barriers and (iii) gate controlled barriers. (i) is not pursued as it was not compatible with BSI, and required a epi not frequently used with CMOS. (ii) offers best FF and frequently preferred [33, 34], but is not chosen due to limited tune-ability and also due to high-electric field concerns in implementations with thinner oxides. Despite the FF and interconnect complexity disadvantages, we opted to utilize approach (iii) with additional barrier electrode in the unit cell, as both of these limitations will be relaxed with BSI.

Two sensors were designed, with 10x10 um^2 and 26x26 um^2 unit cells organized in 128x40 format using four-phase clocking. An additional sensor with 40+ unit cell variations is designed to optimize the pixel layout and conversion gain. One half of all sensors included AB functionality. The CCD core is made up of an active area surrounded with light shielded transition electrodes, which are used to implement the CCD/CMOS transition described above. Additional shielded black-reference columns, and buffer rows/columns with special layout structures are also implemented. One end of the CCD columns is coupled to floating diffusion electrometers. The other end is used either as sink or for electrical charge injection.

A selectable number of stages is typically utilized in aerospace applications to maintain target SNR under changing illumination. The implemented sensors include eight selectable stages. Photo-generated carriers in the unused stages must be removed to prevent them from blooming. This can be accomplished by clocking the unwanted charge in opposite direction to a sink [35], or dumping it to a vertical [36] or lateral [37] AB drain. We utilized the former approach as half of the test array did not included AB function.

For large TDI sensors, other design considerations include ensuring target time constants for electrodes which requires appropriate metal strapping of electrodes [36, 38] and channel stops [7]. It is also important to capture all capacitances in the unit cell, as fringing capacitance between tightly spaced gates and metal straps can be non-ignorable, especially for large arrays. We used field-solvers [39] to capture these items. Additionally, overflow device diffusion must be sized and doped to maintain proper barrier under worst case illumination [33].

The TDI sensor resolution can be improved via optimized zero-wafer/epi selection. For the sensors, we utilized different starting materials one of which is the graded-epi. This epi enables the combination of good red response (thanks to its thickness) and good crosstalk (MTF) (thanks to the graded epi) [40]. Since these wafers have not been previously used with CMOS technology, we performed TCAD studies to study device isolation, latch-up, PPD and lateral/vertical bipolar devices. Based on these studies, certain layout rules needed to be enforced to ensure reliable CMOS operation.

TDI Sensor CMOS multiplexer: The availability of CMOS allows implementation of sophisticated electrometers (for example CTIAs with adjustable conversion gain), on-sensor ADCs, and clock drivers (for example sub-pixel TDI stage selection). Figure 3 shows the architecture of the TDI sensors. To focus on CCD module integration and process splits, CMOS technology for the prototype sensors was limited to the minimum (single oxide/threshold devices, two metal layers). The readout utilizes column-parallel source followers coupled to switched capacitor sample/hold stages. Two sets of S/H capacitors are used to allow pipe-lined operation, aimed for CCD/CMOS transfer lag measurements. In operation, signal and reset levels are sampled to allow correlated double sampling (CDS), followed by column-by-column readout from a single analog output port using an address-decoder based multiplexer [41]. To allow characterization with wide range of clock shaping options, we opted for off-chip clock drivers.

Radiation Damage Concerns: For space applications, radiation sensitivity of the sensor is a major concern, and should be considered at the architecture, circuit, layout and device/process design levels. For the prototype sensors, we focused on the former three. For typical operating orbits, tolerance to both ionizing and high-energy particles (protons, neutrons) is required [42].

With the relatively thin oxides of the modern CMOS technologies, impact of Vth shifts is expected to be minimal, however field-oxide inversion/leakage is a major concern [43, 44]. On the CMOS electronics, we made extensive utilization of guard-rings both to reduce latch-up risk (which was enhanced for graded-epi wafers) and also to collect field generated leakage. All analog and digital modules used enclosed layout transistors to reduce impact of parasitic leakage paths. Only static logic with relatively larger nodal capacitances is used as a precaution for single events. Since digital logic on the prototype sensor was kept minimal, special logic gates (e.g. upset hardened latches) or additional redundancy are not employed at this time.

For the CCD core, an increased dark-current with ionizing radiation is unavoidable. One countermeasure is to utilize pinning mode to quench surface generation [45]. To reduce the chance of transfer efficiency degradation of smaller charge pockets due to radiation induced bulk-defects, notch-channel CCDs can be used [46]. For the first technology prototypes we did not employ these techniques: Our countermeasures are limited to (1) guard-ring around CCD core to collect field leakage, (2) additional shielded buffer columns around main CCD array, (3) electrical charge injection capability to compensate defect effects via fat-zero approach. In addition to the TDI sensors, the design includes a wide range of test structures to evaluate radiation and latch-up response of the technology. Depending on the radiation response of these structures and prototype sensors, additional countermeasures will be considered for future iterations.

Conclusion: In this paper we described an embedded CCD module integrated into 130nm CMOS/CIS process and prototype TDI sensors utilizing this technology. Both sensors described have been fabricated (Figure 4). Initial channel potential measurements from test structures are close to the design targets. Detailed characterization is currently ongoing.

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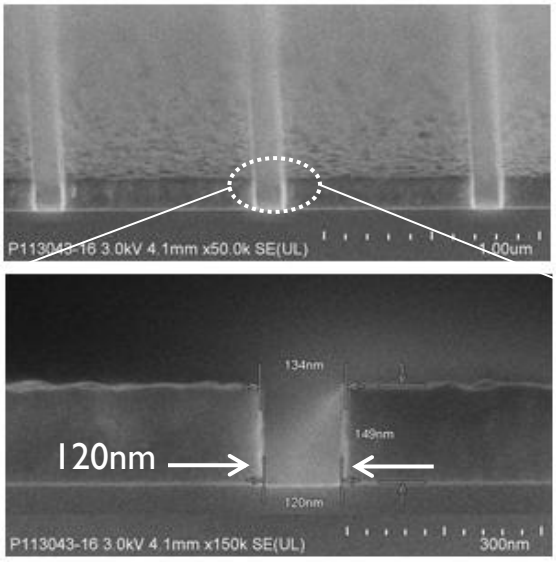

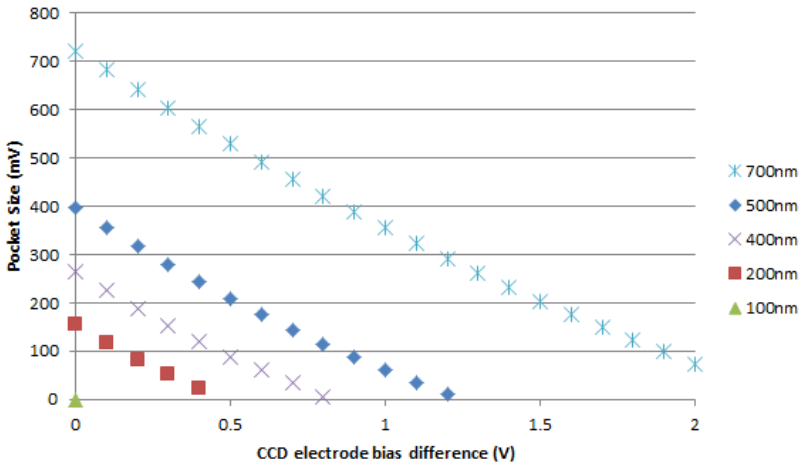

Figure 1 – Top, left shows the narrow gap electrode arrangement for the CCD. Right: inter-electrode pocket size as a function of electrode separation and potential difference (from TCAD).

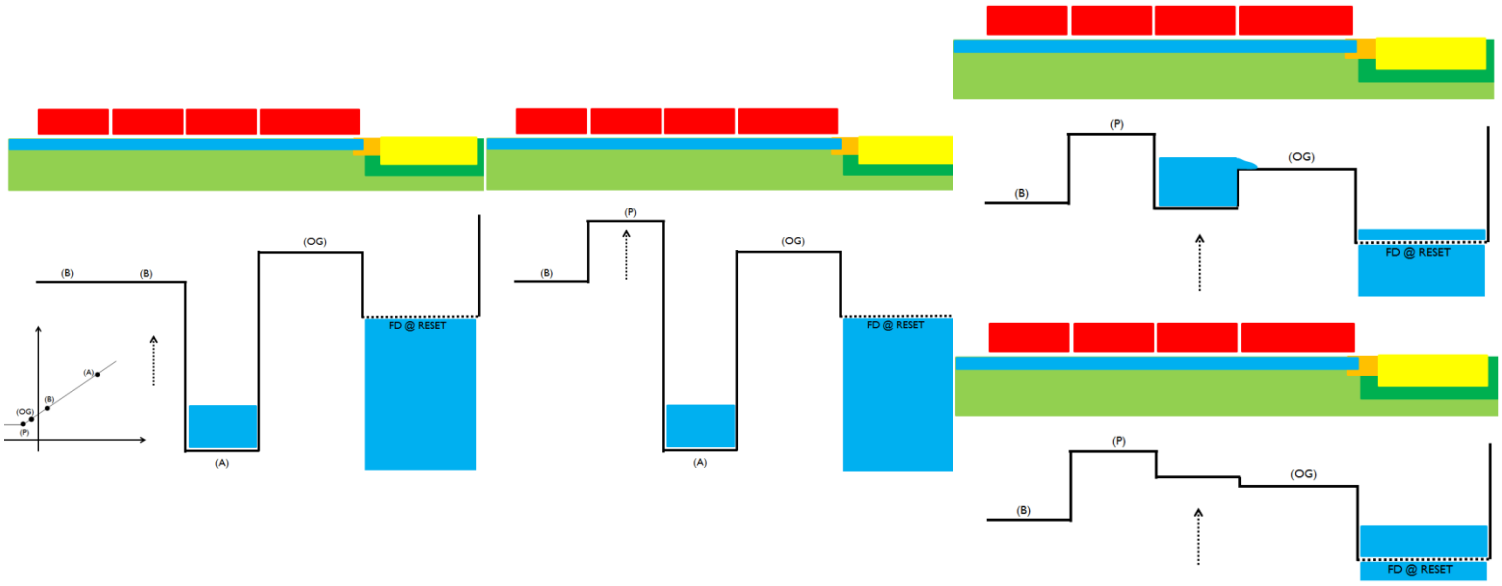

Figure 2 –CCD readout scheme. Inset on first step shows various operating points on electrode vs. channel potential curve.

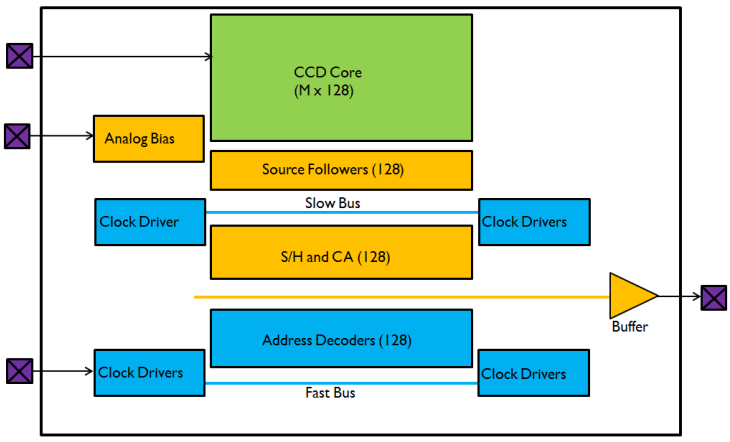

Figure 3 –Simplified block diagram of the TDI sensors

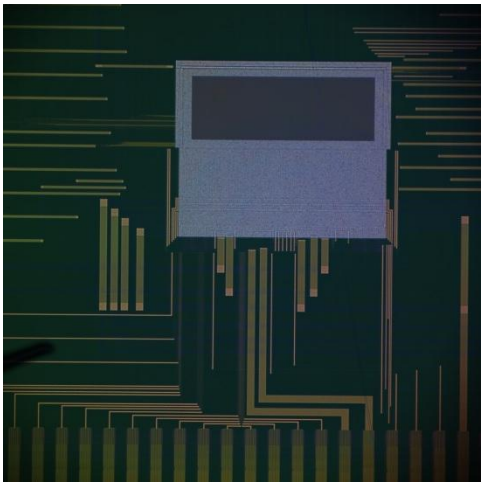

Figure 4 –Top view of one of the fabricated TDI sensors